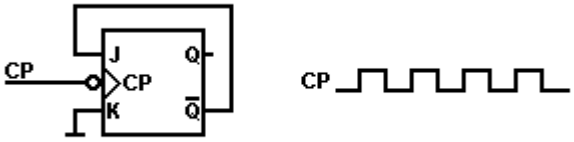
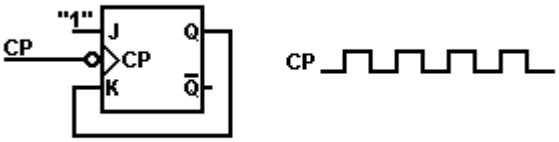
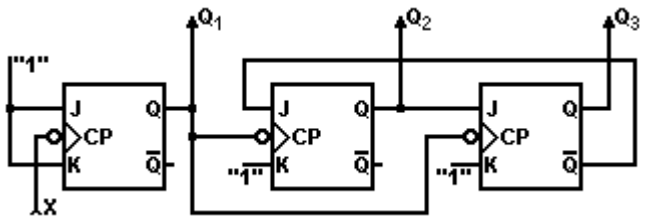
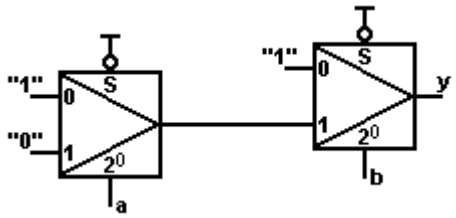
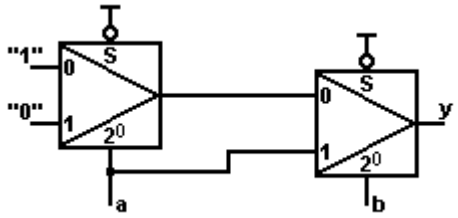
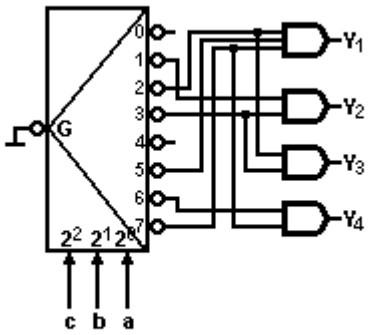
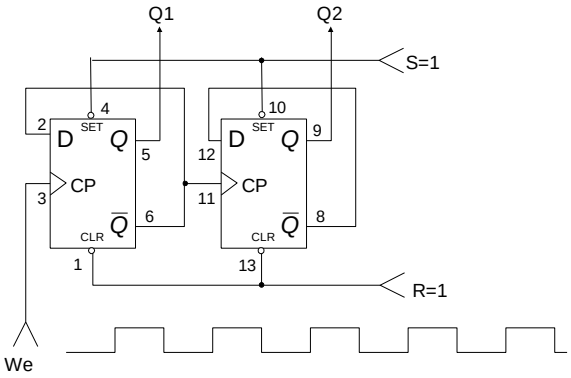
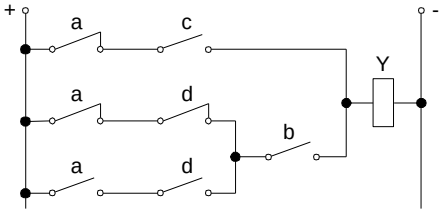
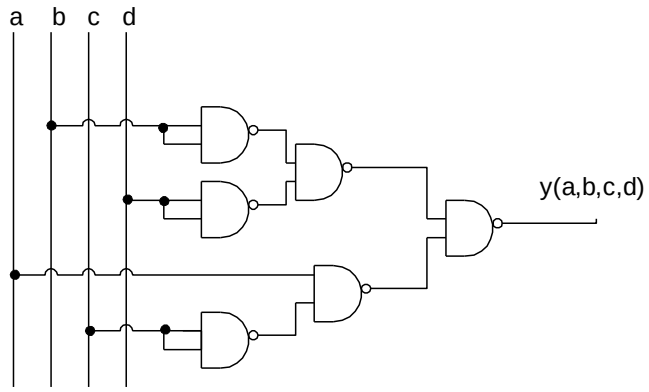
Examination questions on the subject of Digital Technology

Operational level			
Digital Technology			
Questions O/T - means Basic/Advanced			
Item	**O/T**	**Question**	**Correct answer**
1.	O	The JK flip flop switch has been connected according to the shown diagram, assuming that it was zeroed at the initial moment..  System a) modifies its state after each steep sloping clock slope, b) maintains the previous condition, c) switches to state 0 and remains there, d) switches to state 1 and remains there.	D
2.	O	The JK flip flop switch has been connected according to the shown diagram, assuming that it was zeroed at the initial moment..  System a) changes its condition after each descending clock slope, b) maintains the previous condition, c) switches to state 0 and remains there, d) switches to state 1 and remains there.	A
3.	O	Examine a system that performs the following logical function: **Y**(d, c, b, a) = Σ (5, 10, 11, 13, 14, 15). In the system structure, in order to eliminate the possibility of static hazard, the following additional components should be introduced a) d c a, b) $\overline{d}\ c\ a$, c) $d\ \overline{c}\ a$,	A

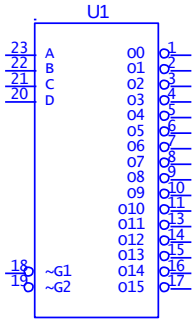
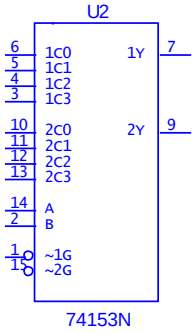
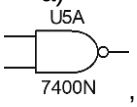
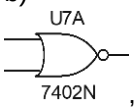
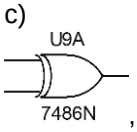
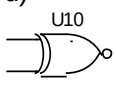
		d) $d\ c\ \bar{a}$.	
4.	O	Assume that $Q_1(0) = Q_2(0) = Q_3(0) = 0$, with Q_1, Q_2, Q_3 having weights of 20,21,22 respectively. The system shown in the figure is:   a) the answers b, c, d are not true, b) the forward counting modulo 7 counter, c) the forward counting in the natural binary code modulo 6 counter., d) the forward counting in the natural binary code modulo 5 counter.	C
5.	O	What function does the system illustrated in the figure perform?  a) the answers b, c, d are not true, b) NAND, c) XNOR, d) XOR.	B

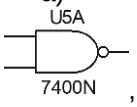
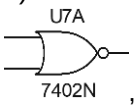
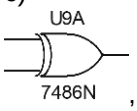
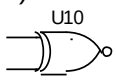
6.	O	What function does the system illustrated in the figure perform?  a) NAND, b) NOR, c) XNOR, d) XOR.	C
7.	O	What function does the system illustrated in the figure perform?  a) $Y_1(a, b, c) = \Pi(2,5,7)$, $Y_2(c, b, a) = \Pi(1,3)$, $Y_3(a, b, c) = \Pi(2,3)$, $Y_4(c, b, a) = \Pi(6,5)$, b) $Y_1(c, b, a) = \Pi(2,5,7)$, $Y_2(c, b, a) = \Pi(1,3)$, $Y_3(c, b, a) = \Pi(2,3)$, $Y_4(c, b, a) = \Pi(6,5)$. c) $Y_1(c, b, a) = \Pi(2,5,7)$, $Y_2(c, b, a) = \Pi(1,3)$, $Y_3(c, b, a) = \Pi(2,3)$, $Y_4(a, b, c) = \Pi(6,5)$.	B

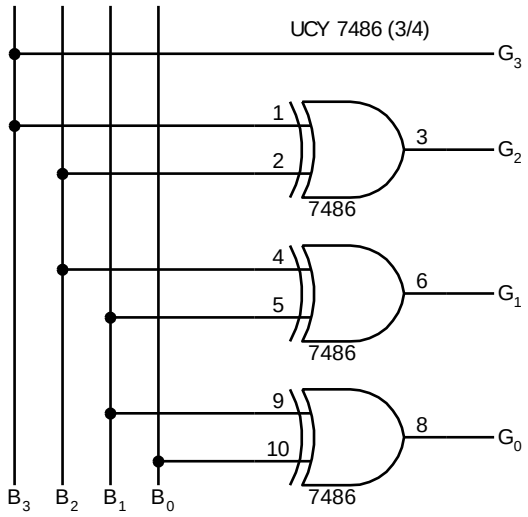
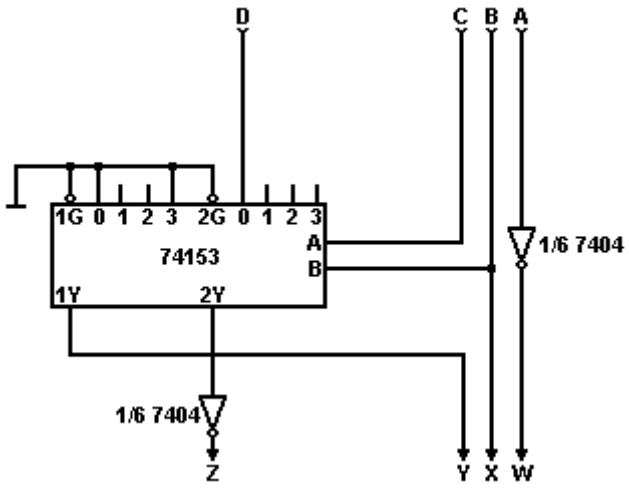
8.	O	Assume that Q1 (0) = Q2 (0) = 0, with Q1, Q2 having weights of 20.21 respectively. The system shown in the figure is:  a) the backwards counting in the natural binary code modulo 4 counter, b) the forward counting in the natural binary code modulo 4 counter, c) the forward counting in the natural binary code modulo 3 counter.	B
9.	O	Specify the Y function of the contact system  a) $\bar{a}\,c+(\bar{a}\,\bar{d}+a\,d)\,b\,c$, b) $\bar{a}\,c+(\bar{a}\,\bar{d}+a\,d)\,c$, c) $\bar{a}\,c+(\bar{a}\,\bar{d}+a\,d)\,b$.	C
10.	O	Determine the signal at the y output.	C

		 a) $\overline{b}\ d + \overline{a}\ c$, b) $b\ \overline{d}\ + \overline{a}\ c$, c) $b\ \overline{d}\ + a\ \overline{c}$.	
11.	O	In the architecture of PLA, the matrix of products and sums meets the following conditions a) the products is programmable, the sums is programmed permanently, b) both matrices are programmable, c) sums is programmable, the products are programmed permanently.	B
12.	O	The number 46 $_{10}$ in the hexadecimal code should be recorded as a) 3 E H, b) 2 F H, c) 2 E H.	C
13.	O	The number 378 $_{10}$ in the BCD code is recorded as a) (0011 0111 1010) $_{BCD}$, b) (0011 0111 1000) $_{BCD}$, c) (0111 0011 1000) $_{BCD}$.	B
14.	O	The sum of the numbers 10111011_2 and 10111_2 shall be as follow a) 11110010_2, b) 11010010_2, c) 10110010_2.	B

15.	O	The number **+21$_{10}$** in 8-bit code completion to 2 (U2) should be written as a) 00010101 U2, b) 10010101 U2, c) 00110101 U2.	A
16.	O	The number **+21$_{10}$** in 8-bit code module character (ZM) is written as a) 00010101 ZM, b) 10010101 ZM, c) 00110101 ZM.	A
17.	O	The number **+21$_{10}$** in 8-bit code of the completion code up to 1 (U1) is written as a) 00010101 U1, b) 10010101 U1, c) 00110101 U1.	A
18.	O	The function performed by the EXCLUSIVE OR (EX OR) 2-way gateway can be written as a) Y=f(a, b) = $a+b$, b) Y=f(a, b) = $=a\bar{b}+\bar{a}b$, c) Y=f(a, b) = $=\bar{a}\bar{b}+ab$.	B
19.	O	The function performed by the EXCLUSIVE OR (EX OR) 2-way gateway can be written as a) Y=f(a, b) = $\overline{a \oplus b}$ b) Y=f(a, b) = $a \oplus b = a \otimes b$, c) Y=f(a, b) = $a \oplus b = \overline{a \otimes b}$.	C
20.	O	The function performed by the EXCLUSIVE NOR (EX NOR) 2-input gateway can be written as a) Y=f(a, b) = $a+b$, b) Y=f(a, b) = $=a\bar{b}+\bar{a}b$, c) Y=f(a, b) = $=\bar{a}\bar{b}+ab$.	C

21.	O	What role does the system with the following symbol play  a) demultiplexer with 4 address inputs, at the output 0 is active, b) demultiplexer with 4 address inputs, at the output 1 is active, c) multiplexer with 4 address inputs.	A
22.	O	What does the system with the following symbol contain  a) 2 multiplexers, each with its own 4 information inputs and 2 address inputs, b) 2 multiplexers with 4 information inputs and 2 shared address inputs, c) 2 demultiplexers with 4 address inputs.	B
23.	O	The EXCLUSIVE OR (EX OR) gateway is represented by the following symbol a)  , b)  , c)  , d)  .	C

24.	O	The NOR gateway is represented by the following symbol a)  , b)  , c)  , d)  .	B
25.	O	The following environment is used to prepare digital control algorithms for PLD programmable systems a) BASCOM, b) Delphi, c) Max Plus Baseline and Quartus.	C
26.	O	In PAL architecture, the matrix of the product and sum fulfills the following conditions a) the products is programmable, the sums is programmed permanently, b) both matrices are programmable, c) sums is programmable, the products are pre-programmed permanently.	A

27.	O	The figure shows a diagram of the 4-bit natural binary code translator to the Gray code.  Determine the signal at the outputs of the circuits G_3, G_2, G_1, G_0 when the signal 1 0 0 0 1 is given on the inputs B_3, B_2, B_1, B_0 respectively. a) 1 0 0 1, b) 1 0 1 1, c) 1 0 0 1, d) 1 1 0 1.	D
28.	O	Inputs D, C, B, A have the following weights: 8,4,4,2,1 respectively, whereas addresses inputs A, B of UCY 74153 multiplexer have the following weights: 1,2 respectively.  Determine the signal at the circuit output when the input D, C, C, B, A is given a signal of 1 0 0 0 0. a) 1 0 0 1, b) 1 0 1 1, c) 0 0 0 1, d) 1 1 0 1.	C